Claims:

1. An apparatus for routing electrical signals comprising:

a layered structure comprising at least one signal trace disposed on a first side of an electrically insulating layer, a via electrically connected to said trace, said via having a conductive stub trace electrically connected thereto, and a generally planar electrically conductive layer disposed on a second side of said electrically insulating layer, wherein said stub trace on said first side defines an area on said second side where said electrically conductive layer is absent.

2. An apparatus as recited in claim 1 wherein said electrically insulating layer comprises a first electrically insulting layer and said generally planar electrically conductive layer comprises a first electrically conductive layer and said layered structure further comprises a second electrically insulating layer disposed on a side of said signal trace opposite said first electrically insulating layer and a second generally planar electrically conductive layer is disposed on said second electrically insulating layer on a side opposite said signal trace, wherein said stub trace also defines an area where said second electrically conductive layer is absent.

3. An apparatus as recited in claim 1 comprising a plurality of said vias and a plurality of said stub traces, wherein all of said stub traces define a plurality of said areas on said second side where said electrically conductive layer is absent.

4. An apparatus as recited in claim 3 wherein said area on said second side where said electrically conductive layer is absent is sufficiently large to increase an impedance of said stub traces and sufficiently small to maintain a structural integrity of said layered structure.

5. An apparatus as recited in claim 1 wherein a width of said stub trace is reduced to a minimum width required for an electroplating process.

6. An apparatus as recited in claim 3 wherein a width of at least one of said plurality stub traces is reduced to a minimum width required for an electroplating process.

7. An apparatus as recited in claim 1 wherein substantially all of said electrically conductive layer is absent for a defined width around a perimeter of said layered structure with the exception of a plurality of electrical contacts necessary for an electroplating process.

8. An apparatus as recited in claim 1 wherein said layered structure is an integrated circuit package.

9. An apparatus as recited in claim 1 wherein said layered structure is a printed circuit board.

10. A method for manufacturing a layered structure for routing electrical signals comprising the steps of:

providing a layout for the layered structure having an insulating layer with at least one signal trace, a via, and a stub trace on a first side of said insulating layer, and a generally planar electrically conductive layer disposed on a second side of said insulating layer,

identifying said stub trace,

defining a beneficial portion on said second side based upon a layout of said stub trace where said electrically conductive layer on said second side is to be absent,

modifying said layout according to said step of defining, and

manufacturing said layered structure according to said modified layout.

11. A method for manufacturing a layered structure as recited in claim 10 wherein said layered structure has a plurality of said signal traces, said vias, and said stub traces on said first side of said insulating layer and said step of identifying comprises identifying one or more of said stub traces, and said step of defining further comprises defining said beneficial portion for each one of said one or more stub traces.

12. A method for manufacturing a layered structure as recited in claim 11 wherein said step of identifying comprises locating one or more stub traces that are relatively longer than remaining ones of said stub traces.

13. A method for manufacturing a layered structure as recited in claim 10 and further comprising the step of simulating performance of a signal on a signal trace, said signal having a registration window wherein said step of identifying comprises locating one or more stub traces that are predicted to generate reflections on said signal traces to which they attach that are added to a signal on said signal trace at a time during said registration window.

14. A method for manufacturing a layered structure as recited in claim 10 wherein said beneficial portion is defined by more than one stub trace.

15. A method for manufacturing a layered structure as recited in claim 10 wherein said layered structure is an integrated circuit package.

16. A method for manufacturing a layered structure as recited in claim 10 wherein said layered structure is a printed circuit board.

17. An apparatus for routing electrical signals comprising:
a layered structure comprising at least one signal trace disposed on a first side of an electrically

insulating layer, a via electrically connected to said trace, said via having a conductive stub trace electrically connected thereto, and a generally planar electrically conductive layer disposed on a second side of said electrically insulating layer, and a means for increasing an impedance of said stub trace.

18. An apparatus as recited in claim 17 wherein said means for increasing said impedance of said stub trace attenuates a reflected signal traveling along said stub trace before it mixes with a signal at said via.

19. An apparatus as recited in claim 17 wherein said mean for increasing said impedance of said stub traces comprises creating a gap in said electrically conductive layer closest to said stub trace.

20. An apparatus as recited in claim 17 wherein said means for increasing said impedance of said stub traces comprises creating a insulating perimetrical portion of said electrically conductive layer having one or more electrical access lines from an edge of said apparatus to said electrically conductive layer.

21. An apparatus as recited in claim 17 wherein said means for increasing said impedance of said stub traces comprises reducing a width of said stub trace relative to a width of a signal trace to which said stub trace is electrically connected.